

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant

Sunil Talwar et al.

LOGIC CIRCUIT AND METHOD FOR CARRY AND SUM GENERATION AND METHOD
OF DESIGNING SUCH A LOGIC CIRCUIT

Docket No.: 1365.063US1
Filed: November 14, 2003
Examiner: Unknown

Serial No.: 10/714408
Due Date: N/A
Group Art Unit: Unknown

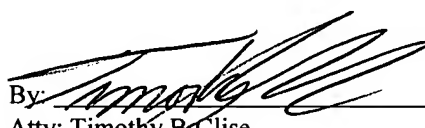
Commissioner for Patents
P.O. Box 1450
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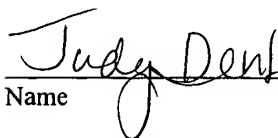
- ☒ A return postcard.
- ☒ A Communication Concerning Related Applications (1 pg.).
- ☒ An Information Disclosure Statement (2 pgs.), Form 1449 (3 pgs.), copies of 34 of the 65 cited documents. Copies include 11 foreign patent documents and 23 publications (other documents).

If not provided for in a separate paper filed herewith, Please consider this a PETITION FOR EXTENSION OF TIME for sufficient number of months to enter these papers and please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
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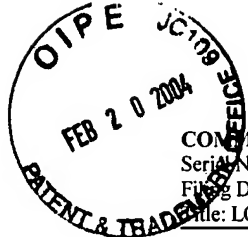
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SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
(GENERAL)



COMMUNICATION CONCERNING RELATED APPLICATIONS

Serial Number: 10/714408

Filing Date: November 14, 2003

Title: LOGIC CIRCUIT AND METHOD FOR CARRY AND SUM GENERATION AND METHOD OF DESIGNING SUCH A LOGIC CIRCUIT

Page 2

Dkt: 1365.063US1

60/473204	May 23, 2003	1365.067PRV	PASS-GATE FULL ADDER WITH FAST CARRY-IN
10/472658	September 22, 2003	1365.072US1	A MULTIPLICATION LOGIC CIRCUIT
10/755723	January 12, 2004	1365.067US1	A SUM BIT GENERATION CIRCUIT
10/757712	January 14, 2004	1365.064US1	A LOGIC CIRCUIT

Respectfully submitted,

SUNIL TALWAR ET AL.

By Applicants' Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 349-9587

Date

17 Feb '04

By

Timothy B. Clise
Reg. No. 40,957

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Judy Dent
Name

Signature



SN 10/714408

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Sunil Talwar et al.	Examiner:	Unknown
Serial No.:	10/714408	Group Art Unit:	Unknown
Filed:	November 14, 2003	Docket:	1365.063US1
Title:	LOGIC CIRCUIT AND METHOD FOR CARRY AND SUM GENERATION AND METHOD OF DESIGNING SUCH A LOGIC CIRCUIT		

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicants respectfully request that this Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicants request that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicants with the next official communication.

Pursuant to 37 C.F.R. §1.97(b), it is believed that no fee or statement is required with the Information Disclosure Statement. However, if an Office Action on the merits has been mailed, the Commissioner is hereby authorized to charge the required fees to Deposit Account No. 19-0743 in order to have this Information Disclosure Statement considered.

INFORMATION DISCLOSURE STATEMENT

Serial No :10/714408

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Title: LOGIC CIRCUIT AND METHOD FOR CARRY AND SUM GENERATION AND METHOD OF DESIGNING SUCH A LOGIC CIRCUIT

Page 2

Dkt: 1365.063US1

The Examiner is invited to contact the Applicants' Representative at the below-listed telephone number if there are any questions regarding this communication.

The present application is either a U.S. national patent application filed after June 30, 2003 or an international application that entered the national stage under 35 U.S.C. § 371 after June 30, 2003. Thus, Applicant believes that the U.S. Patent & Trademark Office has waived the requirement under 37 C.F.R. 1.98 (a)(2)(i) for submitting a copy of each cited U.S. patent and each U.S. patent application publication. The waiver is provided in a pre-OG notice from the U.S. Patent & Trademark Office entitled "Information Disclosure Statements May Be Filed Without Copies of U.S. Patents and Published Applications in Patent Applications filed after June 30, 2003" and dated July 11, 2003. Applicant acknowledges the requirement to submit copies of foreign patent documents and non-patent literature in accordance with 37 C.F.R. 1.98(a)(2).

Respectfully submitted,

SUNIL TALWAR ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 349-9587

Date

17 Feb '04

By

Timothy B Clise
Reg. No. 40,957

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Judith Dent
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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

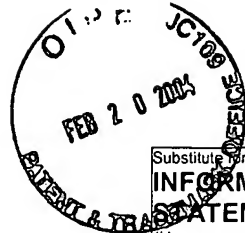
Applicant: Sunil Talwar et al. Examiner: Unknown
Serial No.: 10/714408 Group Art Unit: Unknown
Filed: November 14, 2003 Docket: 1365.063US1
Title: LOGIC CIRCUIT AND METHOD FOR CARRY AND SUM GENERATION
AND METHOD OF DESIGNING SUCH A LOGIC CIRCUIT

COMMUNICATION CONCERNING RELATED APPLICATION(S)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Applicants would like to bring to the Examiner's attention the following related application(s) in the above-identified patent application:

<u>Serial/Patent</u> <u>No.</u>	<u>Filing Date</u>	<u>Attorney Docket</u>	<u>Title</u>
60/439852	January 14, 2003	1365.064PRV	PASS-GATE IMPLEMENTATION OF LARGE COUNTERS
60/436179	December 23, 2002	1365.063PRV	HIGH SPEED ADDER
09/637532	August 11, 2000	1365.033US1	A PARALLEL COUNTER AND MULTIPLICATION LOGIC CIRCUIT
09/769954	January 25, 2001	1365.039US1	A PARALLEL COUNTER AND A MULTIPLICATION LOGIC CIRCUIT
09/898752	July 3, 2001	1365.048US1	MULTIPLICATION LOGIC CIRCUIT
09/917257	July 27, 2001	1365.051US1	A PARALLEL COUNTER AND A LOGIC CIRCUIT FOR PERFORMING MULTIPLICATION
10/027237	December 20, 2001	1365.059US1	LOGIC CIRCUITS FOR PERFORMING MODULAR MULTIPLICATION AND EXPONENTIATION
60/458776	March 28, 2003	1365.066PRV	BOOTH ENCODED PARTITIONED MULTIPLIERS



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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

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Complete if Known

Application Number 10/714408

Filing Date November 14, 2003

First Named Inventor Talwar, Sunil

Group Art Unit Unknown

Examiner Name Unknown

Sheet 1 of 3

Attorney Docket No: 1365.063US1

US PATENT DOCUMENTS

Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	Filing Date If Appropriate
	US-2001/0010051	07/26/2001	Oberman, Stuart , et al.	708	502	02/12/2001
	US-2002/0026465	02/28/2002	Rumynin, D , et al.	708	210	01/25/2001
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	US-3,634,658	01/11/1972	Brown, Richard	235	92LG	03/19/1970
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FOREIGN PATENT DOCUMENTS

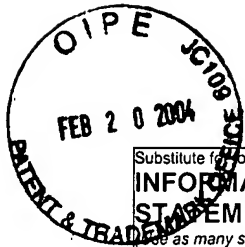
Examiner Initials*	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	T ²
	EP-0168650	01/22/1986	Darringer, J. , et al.	G06F	15/60	
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	EP-0741354	11/06/1996	Ichikawa, Takeshi	G06F	7/50	
	FR-2475250	08/07/1981	Houdard, Jean-Pierre , et al.	606F	7/38	

EXAMINER

DATE CONSIDERED

Substitute Disclosure Statement Form (PTO-1449)

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Application Number 10/714408

Filing Date November 14, 2003

First Named Inventor Talwar, Sunil

Group Art Unit Unknown

Examiner Name Unknown

Sheet 2 of 3

Attorney Docket No: 1365.063US1

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	T ²
	GB-2016181	09/19/1979	Gajski, Daniel	606F	7/39	
	GB-2062310	05/20/1981	Ohhashi, Masahide , et al.	606F	7/52	
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	WO-99/22292	05/06/1999	Verbauwhede, Ingrid			

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

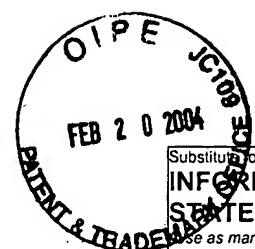
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		BOOTH, ANDREW , "A Signed Binary Multiplication Technique", <u>Oxford University Press, Reprinted from Q.J. Mech. Appl. Math. 4:236-240, (1951),pp. 100-104</u>	
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		FOSTER, CAXTON , et al., "Counting Responders in an Associative Memory", <u>The Institute of Electrical and Electronics Engineers, Inc., Reprinted, with permission, from IEEE Trans. Comput. C-20:1580-1583,(1971),Pgs. 86-89</u>	
		HEKSTRA, et al., "A Fast Parallel Multiplier Architecture", <u>IEEE International Symposium on Circuits and Systems; Institute of Electrical and Electronic Engineers, c1977-c1996, 20v. ill. :28cm, (1992),2128-2131</u>	

EXAMINER

DATE CONSIDERED

Substitute Disclosure Statement Form (PTO-1449)

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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

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Application Number 10/714408**Filing Date** November 14, 2003**First Named Inventor** Talwar, Sunil**Group Art Unit** Unknown**Examiner Name** Unknown

Sheet 3 of 3

Attorney Docket No: 1365.063US1**OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS**

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
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		JONES, ROBERT , et al., "Parallel Counter Implementation", <u>Conf. Rec. 26th Asilomar Conf. Signals, Systems & Computers, Vol. 1, ISBN 0-8186-3160-0,(1992),pp. 381-385</u>	
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EXAMINER**DATE CONSIDERED**

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